REMARKS

Claims 1-23 are pending.

Claims 1, 3, 7, 9-14, 16-17, 20-21 and 23 are objected to.

Claims 8 and 21 are rejected under 35 USC §112, second paragraph.

Claims 1, 7, 8 and 21 are rejected under 35 USC §102(b).

Claims 2-6, 9-19 are rejected under 35 USC §103(a).

Claims 1, 7, 9-14, 16-17, 20-21 and 23 are amended.

New claims 24-26 are added.

No new matter is added.

Claims 3 and 22 are cancelled in favor of amended claims 1 and 21, respectively.

Claims 1-2, 4-21, and 23-26 remain in the case for consideration.

The Examiner has indicated that form 1449 is missing. Applicant hereby submits Form 1449.

Applicant requests reconsideration and allowance of the claims in light of the above amendments and following remarks.

Allowable Subject Matter

Applicant thanks the Examiner's indication that claims 20, 22 and 23 would allowable if re-written in independent form including all of the limitations of the base claim and any intervening claims.

Claim Objections

Claims 1, 3, 7, 9-14, 16-17, 20-21 and 23 are objected to because of inconsistent terminologies. Claims 1, 7, 9-14, 16-17, 20-21 and 23 are amended as suggested by the Examiner. Thus, all of the claim objections are now overcome.

Claim Rejections – 35 USC §112, second paragraph

Claims 8 and 21 are rejected under 35 USC §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 8 and 21 are amended to further clarify the patentable subject matter of the claimed invention. Thus, the rejections of claims 8 and 21 under 35 USC §112 are now overcome.

Claim Rejections – 35 USC §102(b)

Claims 1, 7, 8 and 21 are rejected under 35 USC §102(b) as being anticipated by U.S. Pat. No. 5,981,369 issued to Yoshida, et al. ("Yoshida").

The rejections are respectfully traversed.

Claim 1 is amended to recite,

"exposing the source/drain regions of the first conductive type transistor in the memory cell area and the peripheral circuit area by etching the interlayer insulating layer;

forming first conductive type polysilicon layers on the exposed source/drain regions of the first conductive type transistors;

thereafter, exposing the source/drain regions of the second conductive type transistor in the peripheral circuit area by etching the interlayer insulating layer; and

forming a second conductive type polysilicon layer on the exposed source/drain regions of the second conductive type transistor; and

(e) concurrently forming contact pads on the source/drain regions in the memory cell area and the source/drain regions in the peripheral circuit area."

The Examiner has stated that Yoshida teaches "removing portions of the interlayer insulating layer 16 to form openings (i.e. contact holes) 17-22 that expose the source/drain regions 11, 12/13, 14/15 of the transistors 8A-8C in the memory cell area and the peripheral circuit area (Fig. 8), and filling the openings 17-22 with a conductive material."

Therefore, FIGS. 8 and 9 of Yoshida do not teach the above limitations of the claimed invention, recited in claim 1. In particular, contact holes 17-22 are formed at the same time and plugs 23 are buried in the contact holes 17 to 22 at the same time, unlike the claimed invention recited in claim 1, in which, for example, the source/drain regions of the second conductive type transistor are exposed in the peripheral circuit area *after* forming the first conductive type polysilicon layers.

For these reasons, Yoshida does not teach all of the limitations of claim 1 and, therefore, does not anticipate the claimed invention recited in claim 1. Therefore, claim 1 is now in condition for allowance. Also, claims 7-8, which depend from claim 1 and recite features that are neither taught nor disclosed in the cited references, should also be in condition for allowance.

In addition, claim 21 is amended to recite limitations drawn from allowable claim 22. Thus, claim 21 is allowable.

Claim Rejections – 35 USC §103(a)

Claims 2 and 3 are rejected under 35 USC §103(a) as being unpatentable over Yoshida in view of U.S. Pat. No. 5,949,110 issued to Arima ("Arima").

Claims 4-6 are rejected under 35 USC §103(a) as being unpatentable over Yoshida in view of U.S. Pat. App. Pub. 2002/0014648 to Mizutani, et al. ("Mizutani").

Claims 9-15 are rejected under 35 USC §103(a) as being unpatentable over Yoshida in view of U.S. Pat. No. 6,417,534 issued to Nakahata et al ("Nakahata").

Claims 16-19 are rejected under 35 USC §103(a) as being unpatentable over Yoshida in view of U.S. Pat. No. 6,137,133 issued to Kauffman et al ("Kauffman").

The rejections are respectfully traversed.

Claim 2 depends on claim 1, which is amended hereby. Thus, claim 2 is allowable.

Claim 3 is cancelled in favor of amended claim 1. Thus, the rejection of claim 3 under 35 USC §103(a) is now moot.

Claims 4-6, which depend from claim 1 and recite features that are neither taught nor disclosed in the cited references, should also be in condition for allowance.

With respect to claims 9-15, the Examiner has stated that Nakahata teaches forming a conductive epitaxial silicon layers 20a and 20b on the bottom of the contact holes 18a and 19a, which extend from the source/drain regions onto the isolation layers 2a. However, the conductive epitaxial silicon layers 20a and 20b of Nakahata do not extend from the source/drain regions *onto the isolation layer* 2a. Compare elements 20a and 20b of Nakahata (FIG. 5) with conductive epitaxial silicon layers E_N of the present application. Also see page 13, lines 17-29 of the present application.

Thus, claim 9 is in condition for allowance. Also, claims 10-15, which depend from claim 9 and recite features that are neither taught nor disclosed in the cited references, should also be in condition for allowance.

With respect to claims 16-19, the Examiner has admitted that Yoshida does not teach "implanting first and second conductive type impurities into the opening of the interlayer insulating layer. Instead, first and second conductive type impurities are implanted before forming the openings." The Examiner has, however, argued that Kauffman teach implanting impurities into the openings of the insulating layers 42 (FIG. 6) and 54 (FIG. 10) to form source/drain regions 44 and 60.

Conversely, element 42 is not an interlayer insulating as in the claimed invention, but just a photoresist. See col. 5, lines 48-60.

Accordingly, none of the cited references, either alone or in combination, do not teach or suggest all of the limitations of claim 16. Therefore, the rejection has not presented a prima *facie* case of obviousness. Thus, claim 16 is allowable. Also, claims 17-19, which depend from claim 16 and recite features that are neither taught nor disclosed in the cited references, should also be in condition for allowance.

For the foregoing reasons, reconsideration and allowance of claims 1-2, 4-21, and 23-26 of the application as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

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Respectfully submitted,

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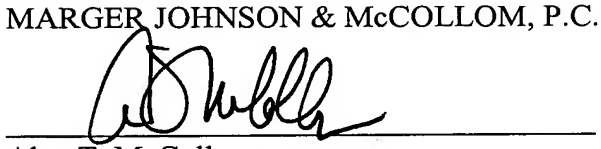

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